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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,433	06/23/2003	Peter T. Sleeman	DYOUP0250US	7155

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EXAMINER	
SHIN, CHRISTOPHER B	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,433	SLEEMAN, PETER T.	
	Examiner	Art Unit	
	Christopher B Shin	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakashima (6,182,204) in view of Jones et al. (5,623,637).

a. Before examiner begin discussing details of art rejection, the examiner would like to point out that:

- Nakashima reference is the primary reference and Jones are secondary references that disclose some of well known/commonly-practiced technique/teachings in the art.
- The examiner also relies on the applicant admitted prior art disclosed in the BACKGROUND OF THE INVENTION section & examiner cited references.
- Examiner would like to point out that the teachings of figures 7-8, in view of well known teachings of figures 1-6, teaches the basic teachings of the claimed invention & the PCMCIA interface IC (703) clearly includes the CIS structure without expressly teaches the bus decode logic as follows:

Claims 1-13	Nakashima (Figs 7-8)
• A semiconductor package/peripheral device card for use in a peripheral devices card connectable to a bus of a host computer	

- (703) for use in a (720) connectable to a bus of (711)

- non-volatile memory for storing a card information structure
  - feature of (704)
- bus decode logic
  - obvious feature of (703) for properly controlling with Data/Address/Control inputs (Do-Dn, Ao-A9, CONTROL, CE1 & REG)
- semiconductor package/peripheral device card provides functions conformant with a PCMCIA standard
  - feature of (703)
- semiconductor package/peripheral device card is a multi-chip module with the non-volatile memory and the bus code logic being realized in respective first and second chips of the multi-chip module
  - obvious variation of (703)
- non-volatile memory and bus decode logic are realized on a single semiconductor substrate
  - obvious variation of (703) in combination with the teachings of Jones reference
- semiconductor package/peripheral device card further includes circuitry associated with an operating function(s) or cards
  - obvious variation of (703) in combination with the teachings of Jones reference
- circuitry further includes UART operating function
  - obvious variation of (703) in combination with the teachings of Jones reference (230)

b. As for claims 1-6, the Nakashima reference does not expressly teaches the bus decode logic being included in a semiconductor package; however, such difference is obvious variation or addition of Nakashima reference for the following reasons:

i. Looking at the figure 8 of Nakashima, one of ordinary skill in the art can expect some kind of bus decode logic/function from the teachings of Nakashima in order to properly understand/decode the bus information (Do-Dn, Ao-A9, CONTROL, CE1 & REG), even without any other teachings of secondary references

ii. Having **either** a bus decode logic & a non-volatile memory for CIS in one functional unit/chip well known and commonly practiced in the art; see Jones & Anderson, respectively. As can be seen from the Primary & Secondary references, Nakashima clearly teaches a non-volatile memory for CIS being part of a PCMCIA interface & Jones clearly teaches bus decoder being part of the PCMCIA interface. Therefore one skill in the art can easily recognize the benefit of both teachings of well known common knowledge & combine the two in the one single chip. In addition, reduction in size and increased performance is natural progression of computing technology; the examiner takes official notice on such well known motivation and teachings, see one of the examiner-cited references Anderson (5,898,869), column 1, lines 13-18 for such well known motivation in a specific PCMCIA environment.

c. For the above reasons, it would have been obvious at the time the invention was made to one having ordinary skill in the art to combine the Jones and Nakashima references to come up with the claimed inventions, for the reasons stated above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher B Shin whose telephone number is 703-305-9658. The examiner can normally be reached on 6:30-5:00 M,Tu,Th,F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher B Shin
Primary Examiner
Of 2182

June 8, 2004
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